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Fig. 1A

(Background Art)

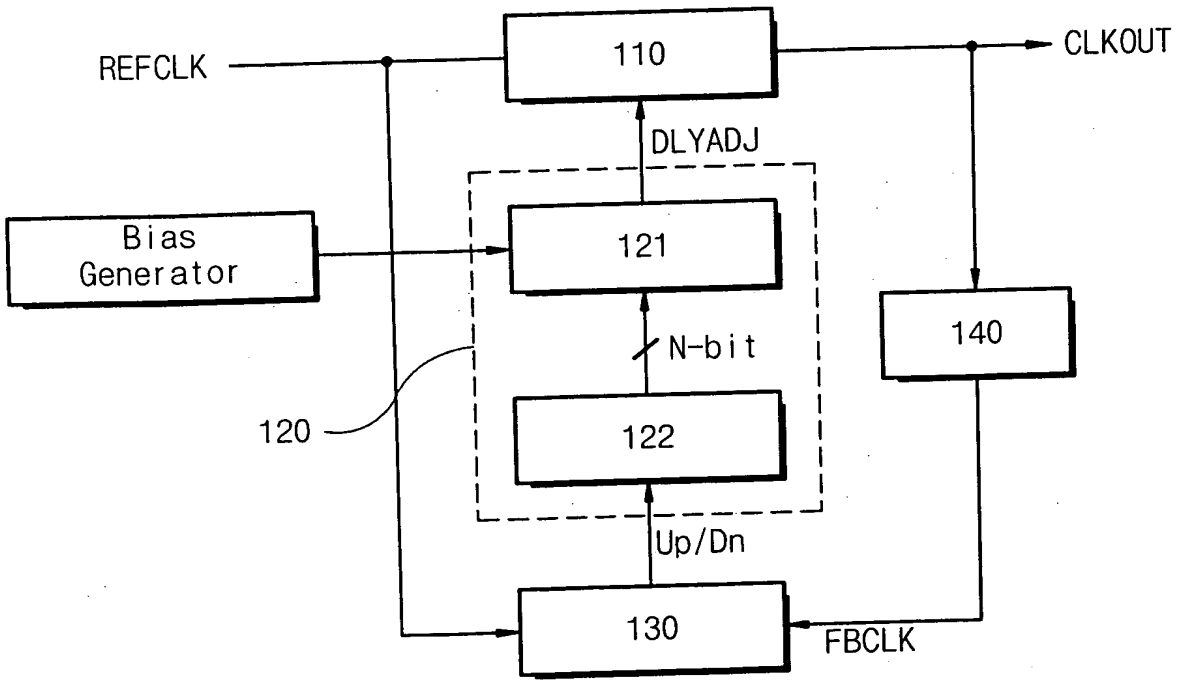


Fig. 1B

(Background Art)

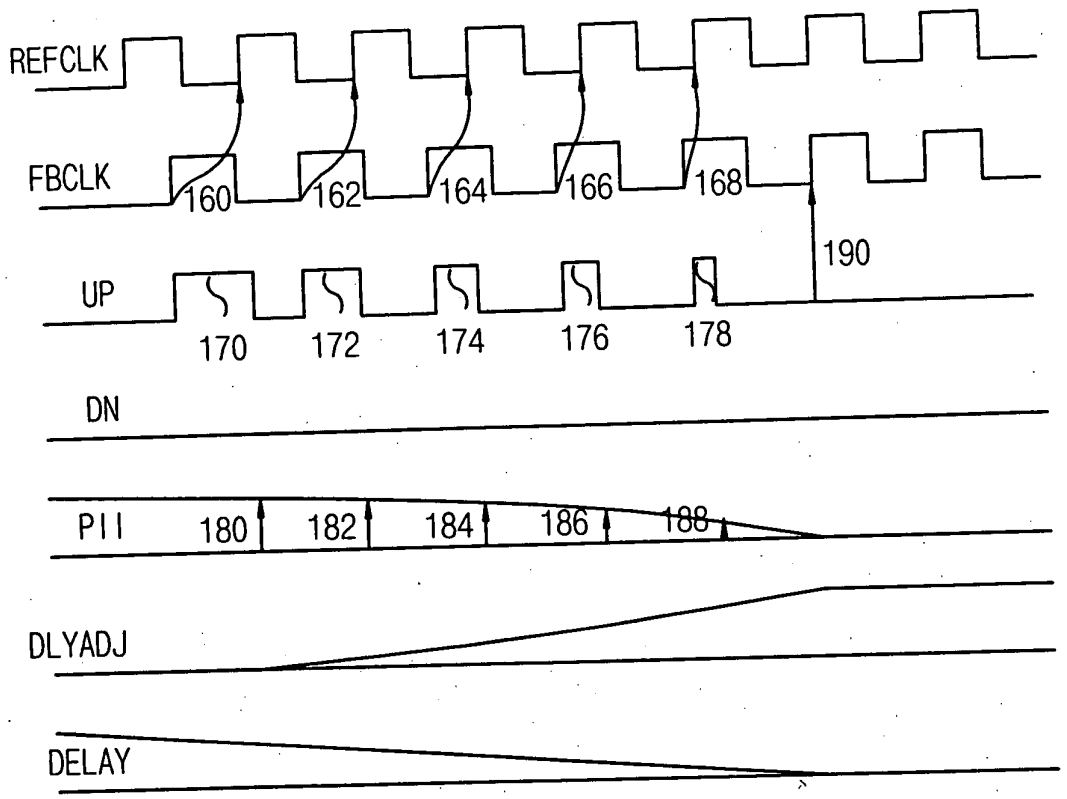


Fig. 2A

(Background Art)

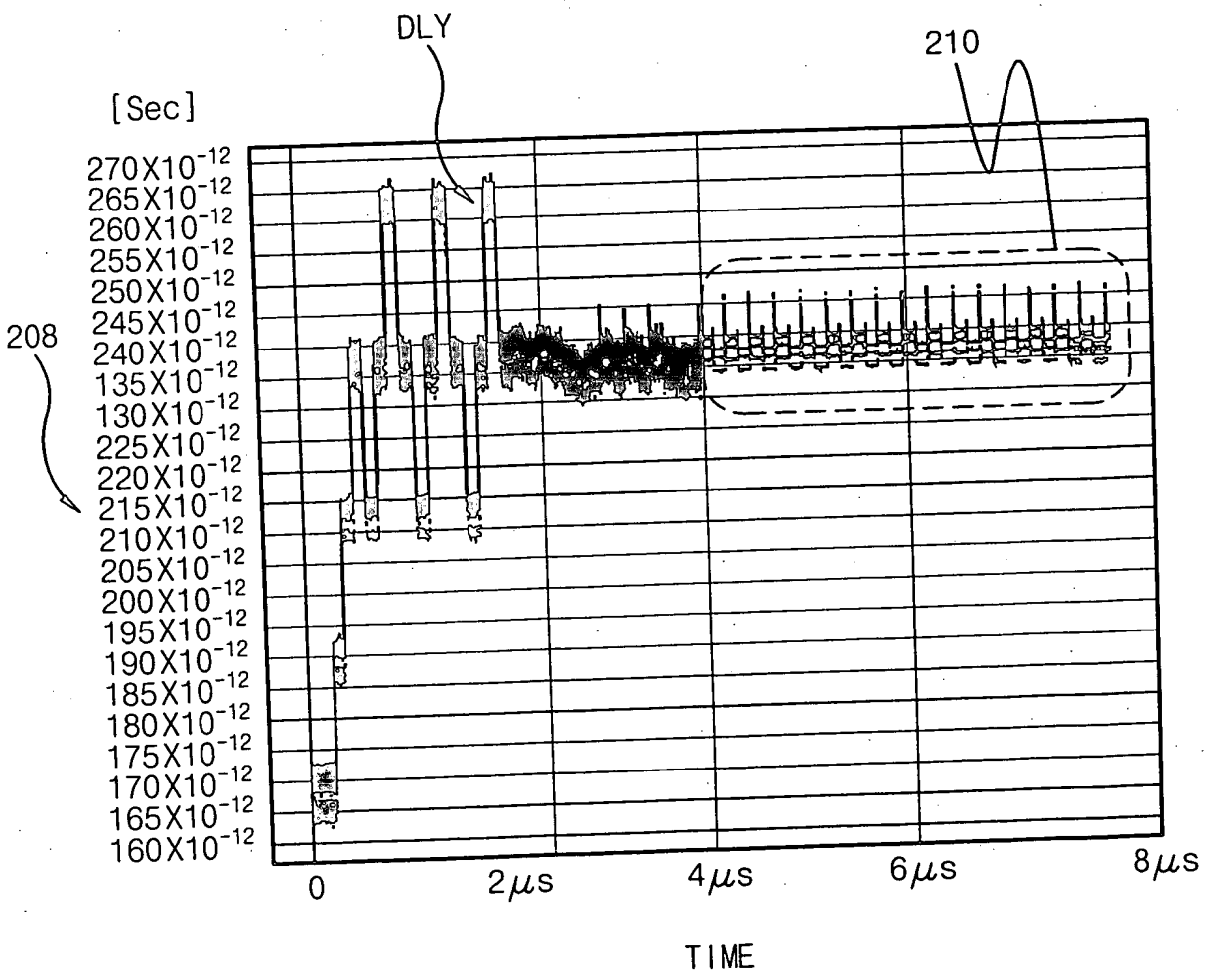


Fig. 2B

(Background Art)

DEC	<-MSB		Binary			LSB->
	B5	B4	B3	B2	B1	B0
30_{10}	0	1	1	1	1	0
31_{10}	0	1	1	1	1	1
32_{10}	1	0	0	0	0	0
33_{10}	1	0	0	0	0	1
34_{10}	1	0	0	0	1	0
33_{10}	1	0	0	0	0	1
32_{10}	1	0	0	0	0	0
31_{10}	0	1	1	1	1	1
30_{10}	0	1	1	1	1	0

Fig. 2C

(Background Art)

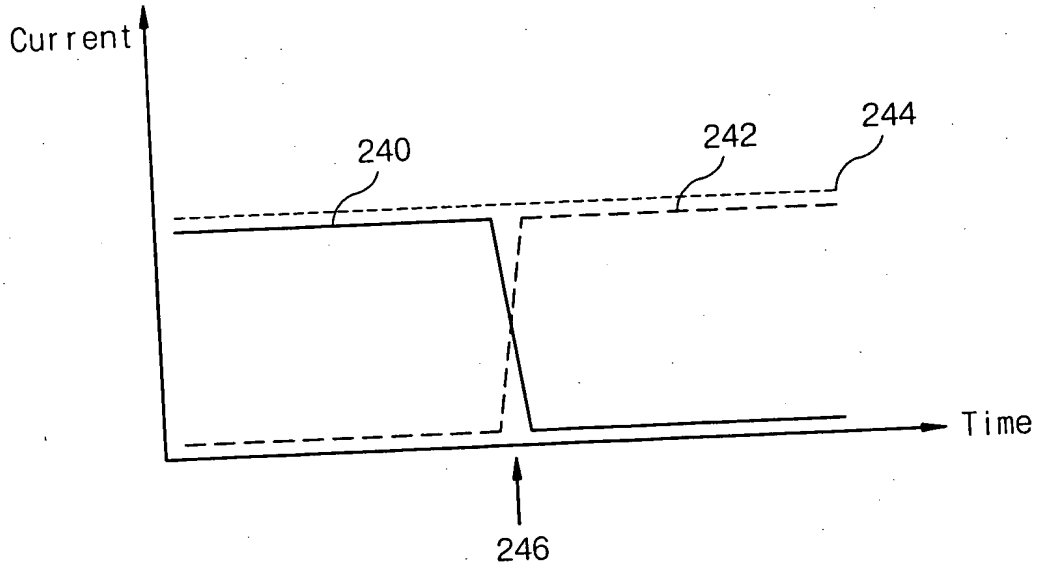


Fig. 2D

(Background Art)

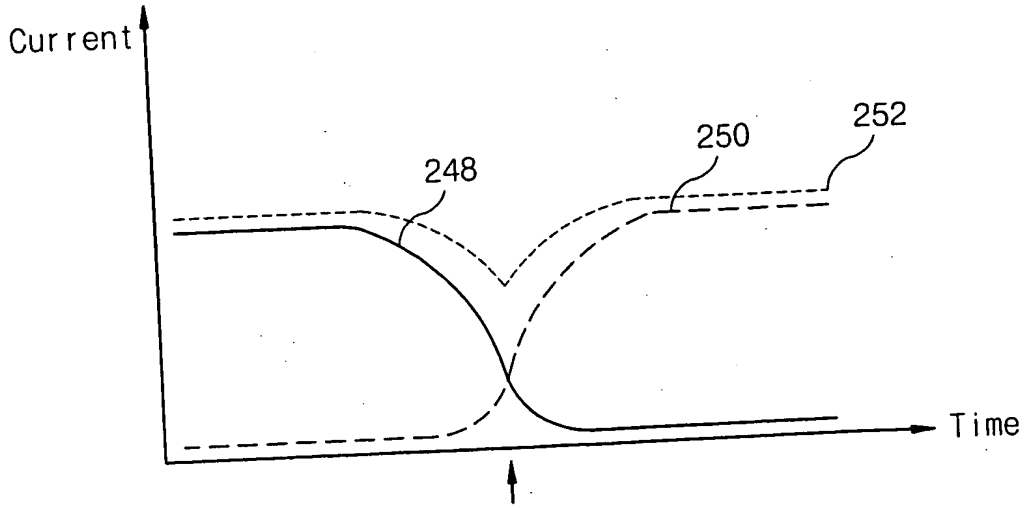


Fig. 3

(Background Art)

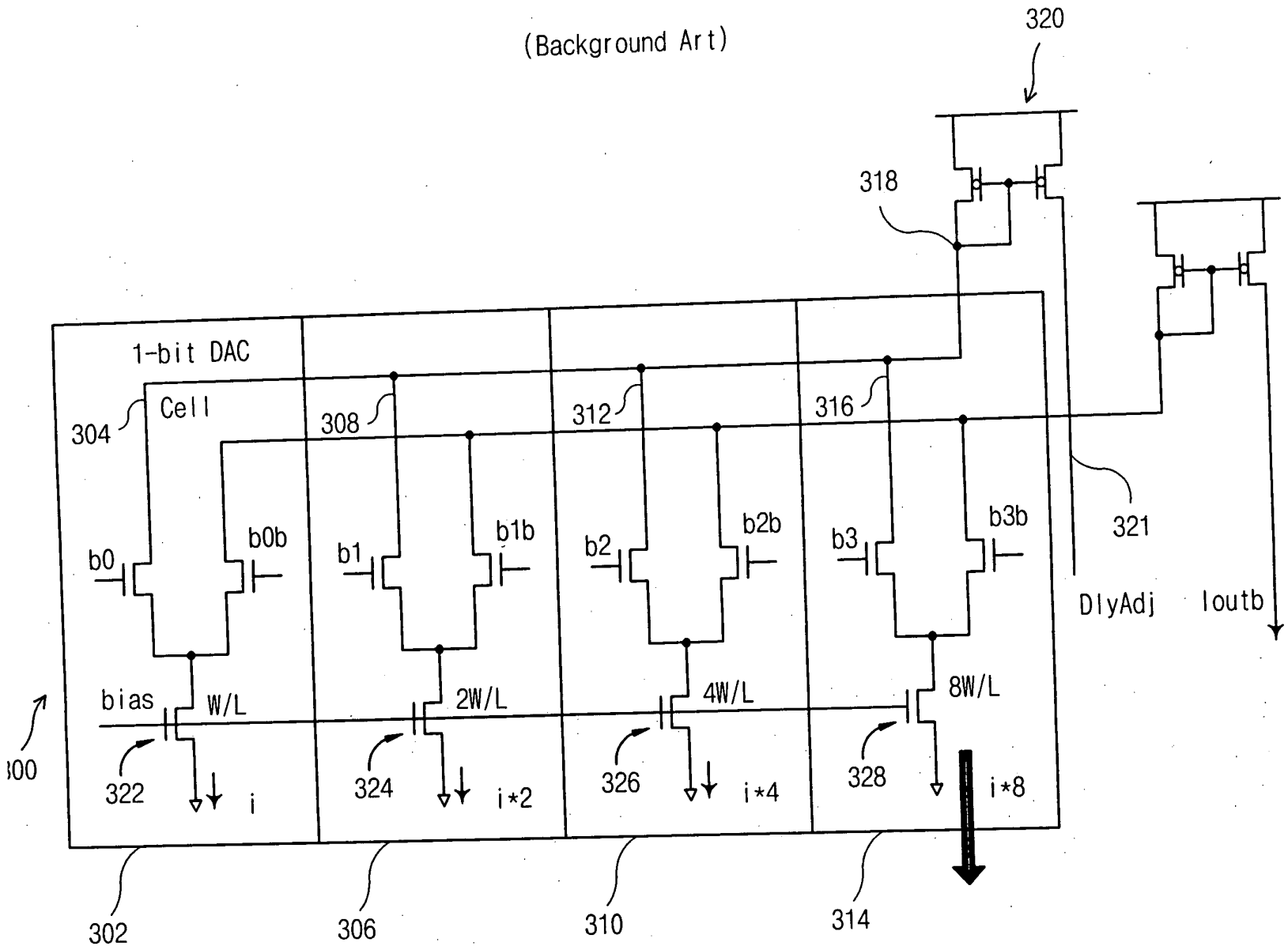


Fig. 4A

(Background Art)

					2_{10}	1_{10}
	4_{10}	4_{10}	4_{10}	4_{10}	2^1	2^0
DEC	b3	b2	b1	b0	C1	C0
0	0	0	0	0	0	0
1	0	0	0	0	0	1
2	0	0	0	0	1	0
3	0	0	0	0	1	1
4	0	0	0	1	0	0
5	0	0	0	1	0	1
6	0	0	0	1	1	0
7	0	0	0	1	1	1
8	0	0	1	1	0	0
9	0	0	1	1	0	1
10	0	0	1	1	1	0
11	0	0	1	1	1	1
12	0	1	1	1	0	0
13	0	1	1	1	0	1
14	0	1	1	1	1	0
15	0	1	1	1	1	1
16	1	1	1	1	0	0
17	1	1	1	1	0	1
18	1	1	1	1	1	0
19	1	1	1	1	1	1

Fig. 4B

(Background Art)

c3	c2	b0	b1	b2	b3
0	0	0	0	0	0
0	1	1	0	0	0
1	0	1	1	0	0
1	1	1	1	1	0

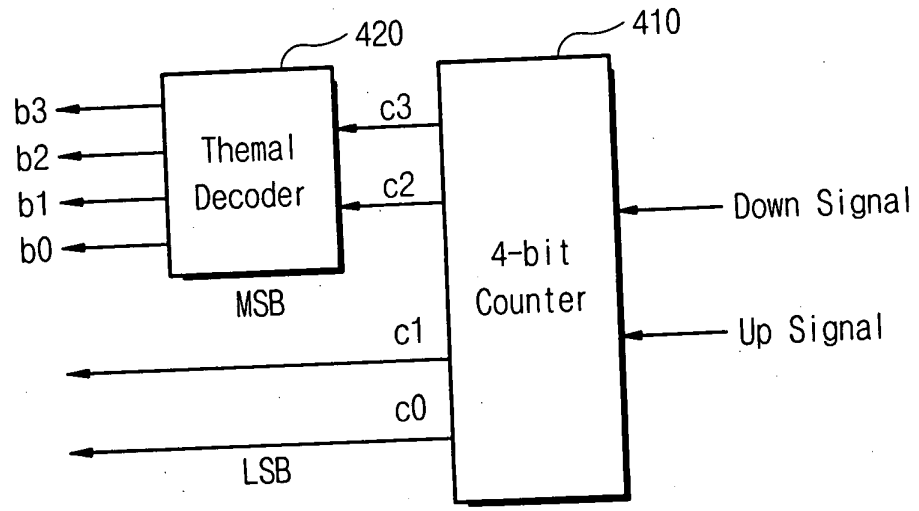


Fig. 4C

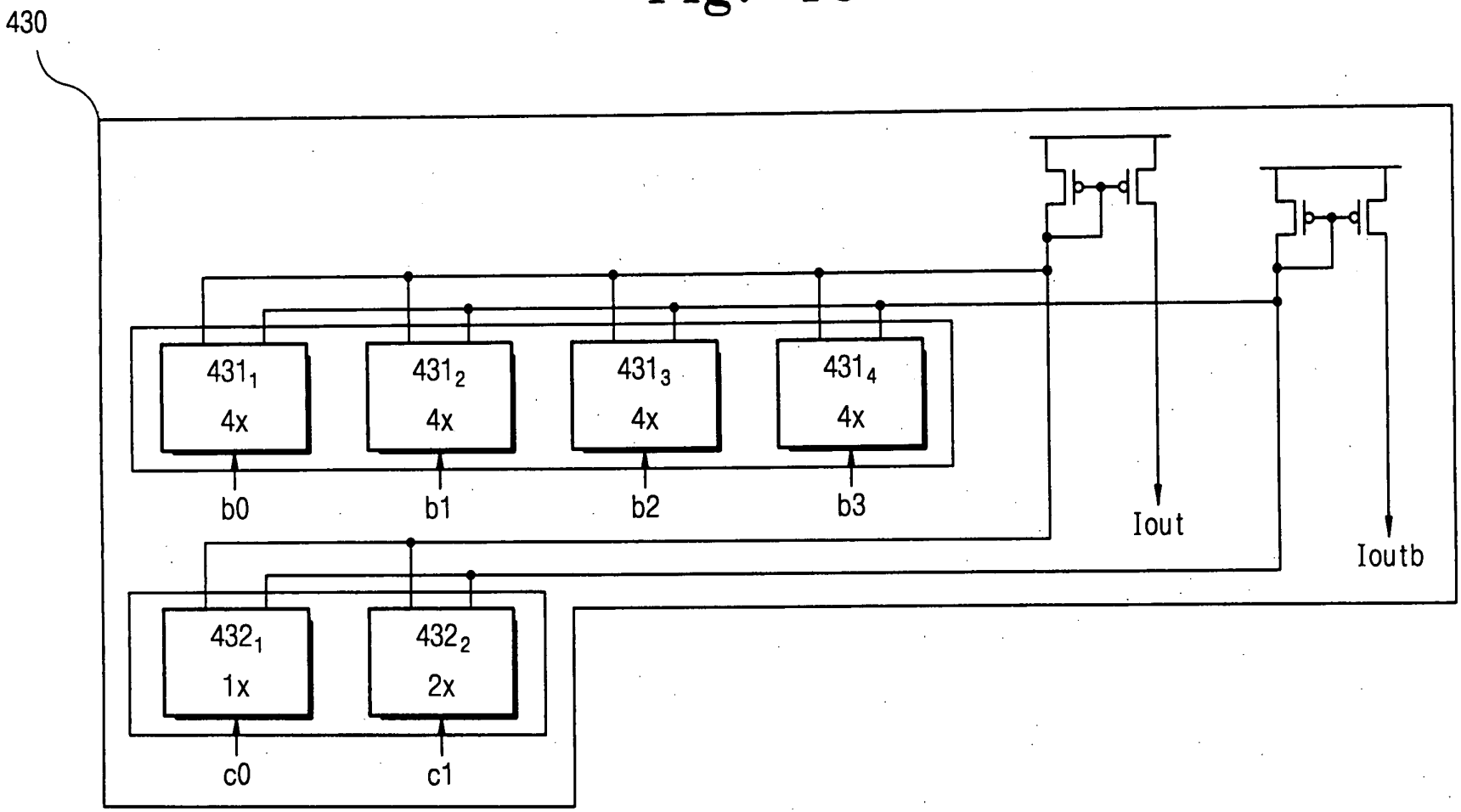

430
431_1
4x
431_2
4x
431_3
4x
431_4
4x
b0
b1
b2
b3
Iout
Ioutb
432_1
1x
432_2
2x
c0
c1

Fig. 5

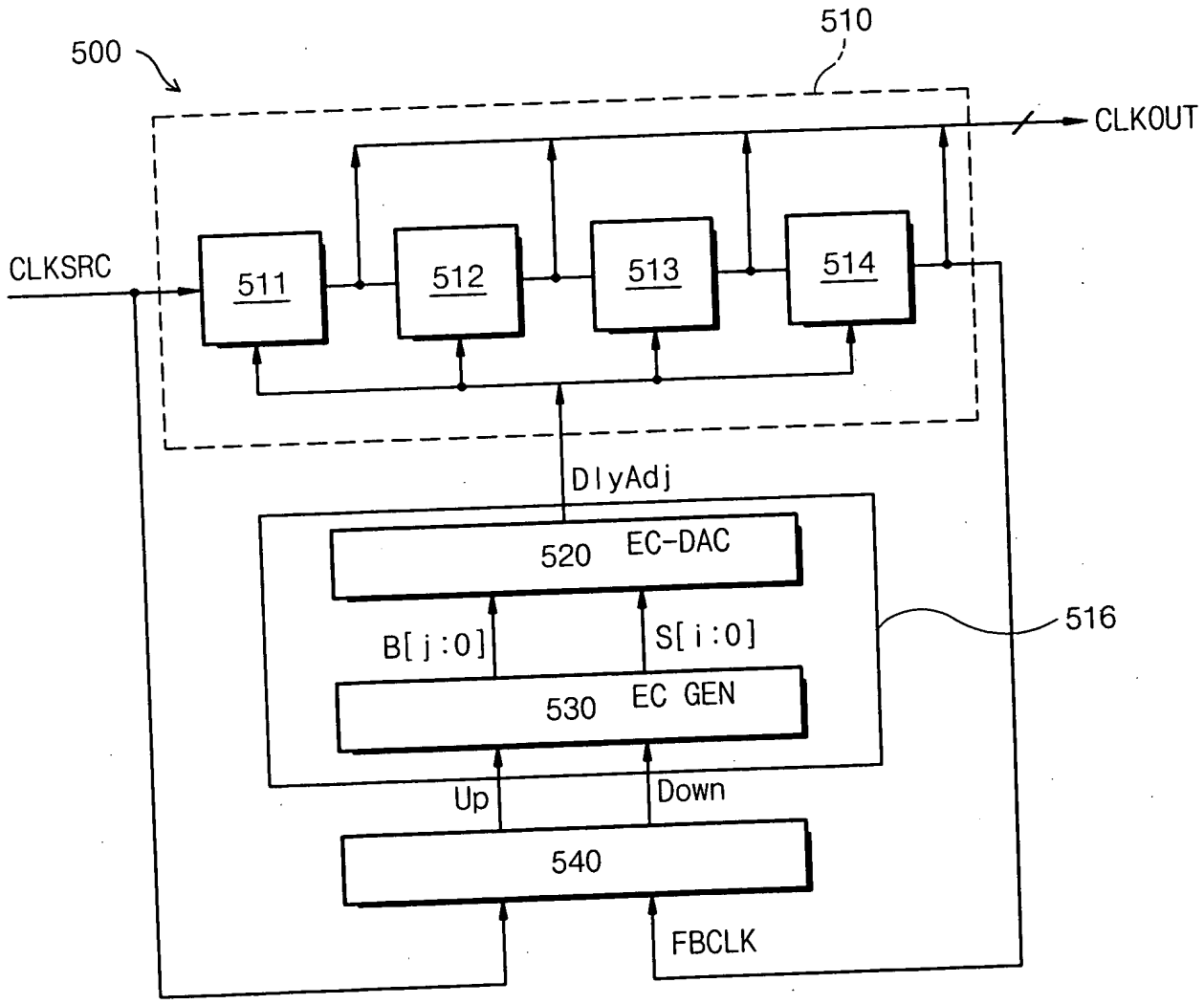

500
510
CLKOUT
CLKSRC
511
512
513
514
DlyAdj
520 EC-DAC
B[j:0]
S[i:0]
530 EC GEN
516
Up
Down
540
FBCLK

Fig. 6A

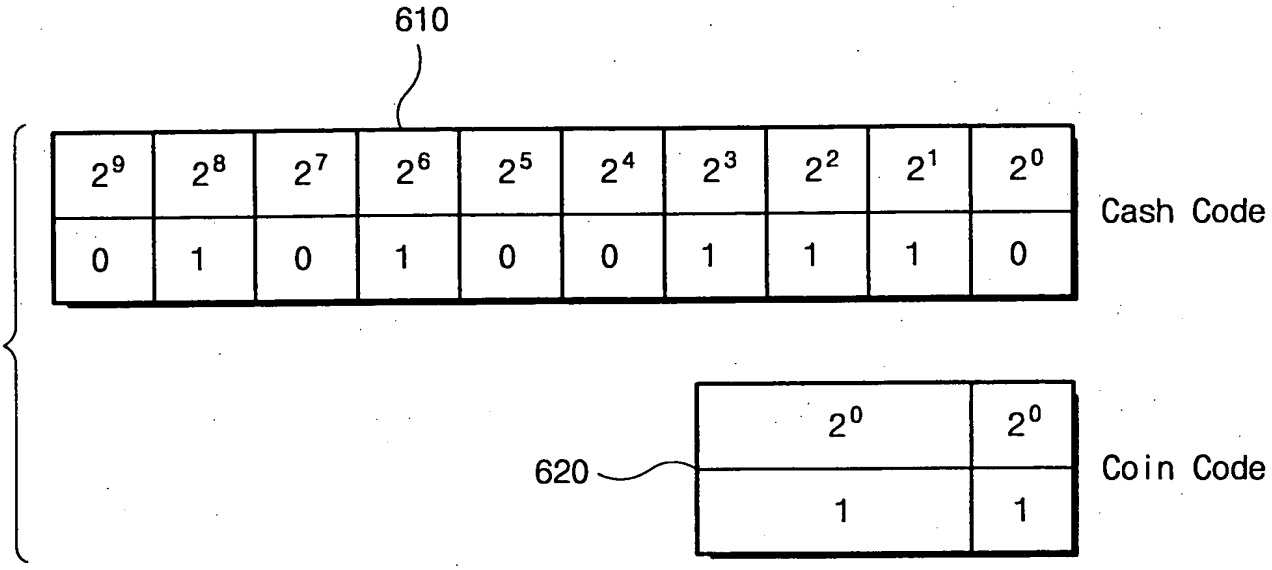


Fig. 6B

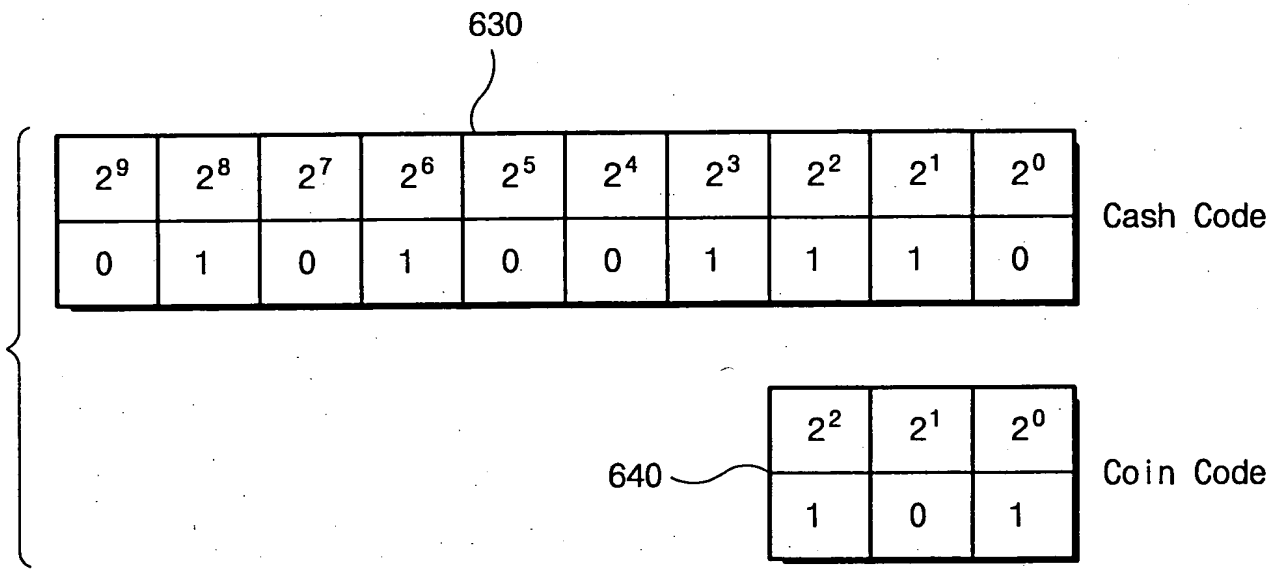


Fig. 6C

$32_{10} = 011110[32] + 00[0]$
$32_{10} = 011100[30] + 11[2]$
$32_{10} = 011101[31] + 01[1]$

Cash Code Coin Code

Fig. 7A

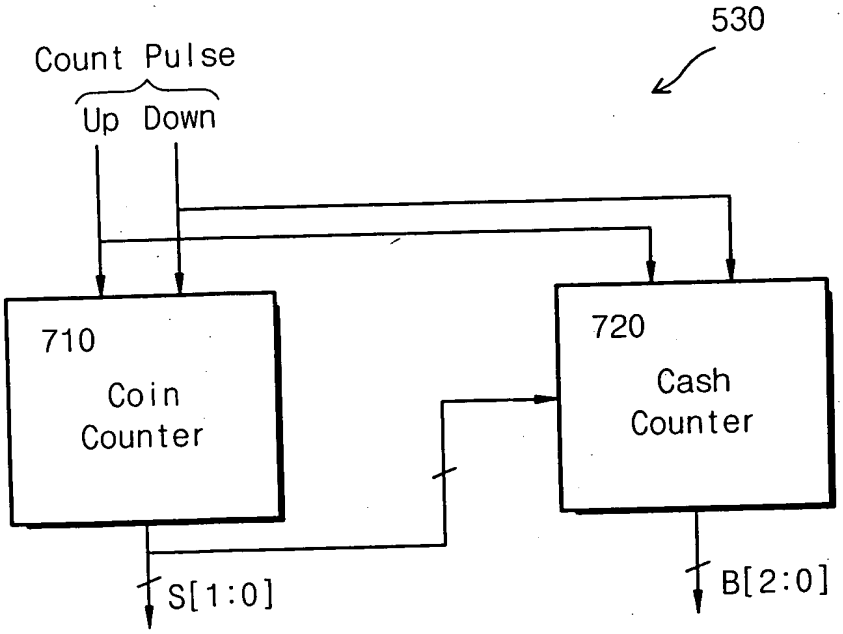

530
Count Pulse
Up Down
710
Coin Counter
720
Cash Counter
S[1:0]
B[2:0]

Fig. 7B

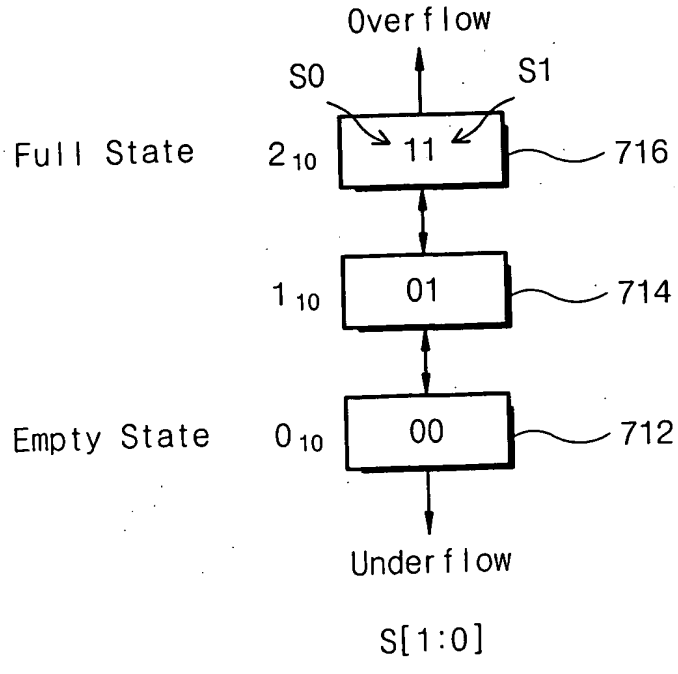

Overflow
S0
S1
Full State
2_{10}
11
716
1_{10}
01
714
Empty State
0_{10}
00
712
Underflow
S[1:0]

Fig. 7D

DEC	$1_{10}1_{10}$ S1S0	64_{10} 2^6 B6	32_{10} 2^5 B5	16_{10} 2^4 B4	8_{10} 2^3 B3	4_{10} 2^2 B2	2_{10} 2^1 B1	1_{10} 2^0 B0	
•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	
31	01	0	0	1	1	1	1	0	
32	11	0	0	1	1	1	1	0	
33	11	0	0	1	1	1	1	1	← 730
34	11	0	1	0	0	0	0	0	← 731
33	01	0	1	0	0	0	0	0	← 732
32	00	0	1	0	0	0	0	0	← 734
33	01	0	1	0	0	0	0	0	← 736
34	11	0	1	0	0	0	0	0	← 738
33	01	1	0	1	0	0	0	0	← 740

Fig. 7C

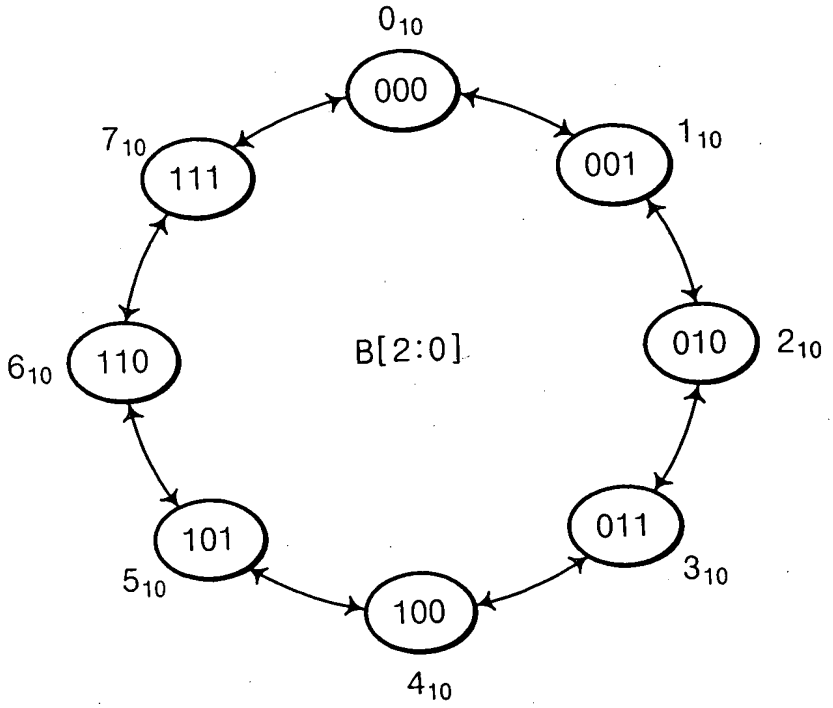
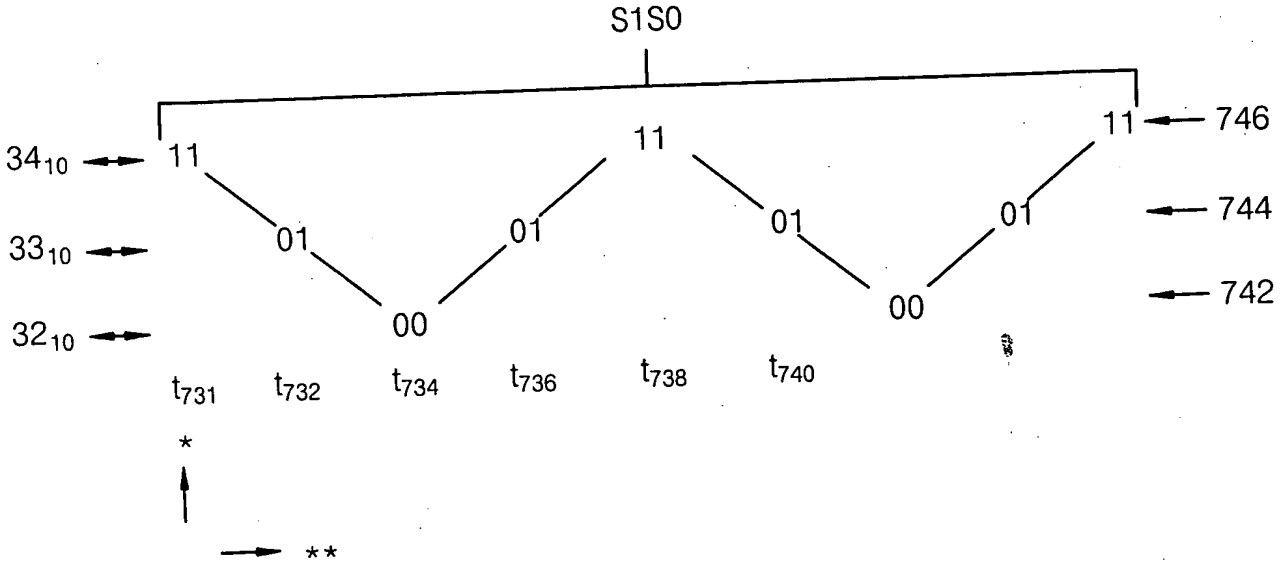


Fig. 7E



* Coin Code Magnitude

** Time, t

Fig. 8

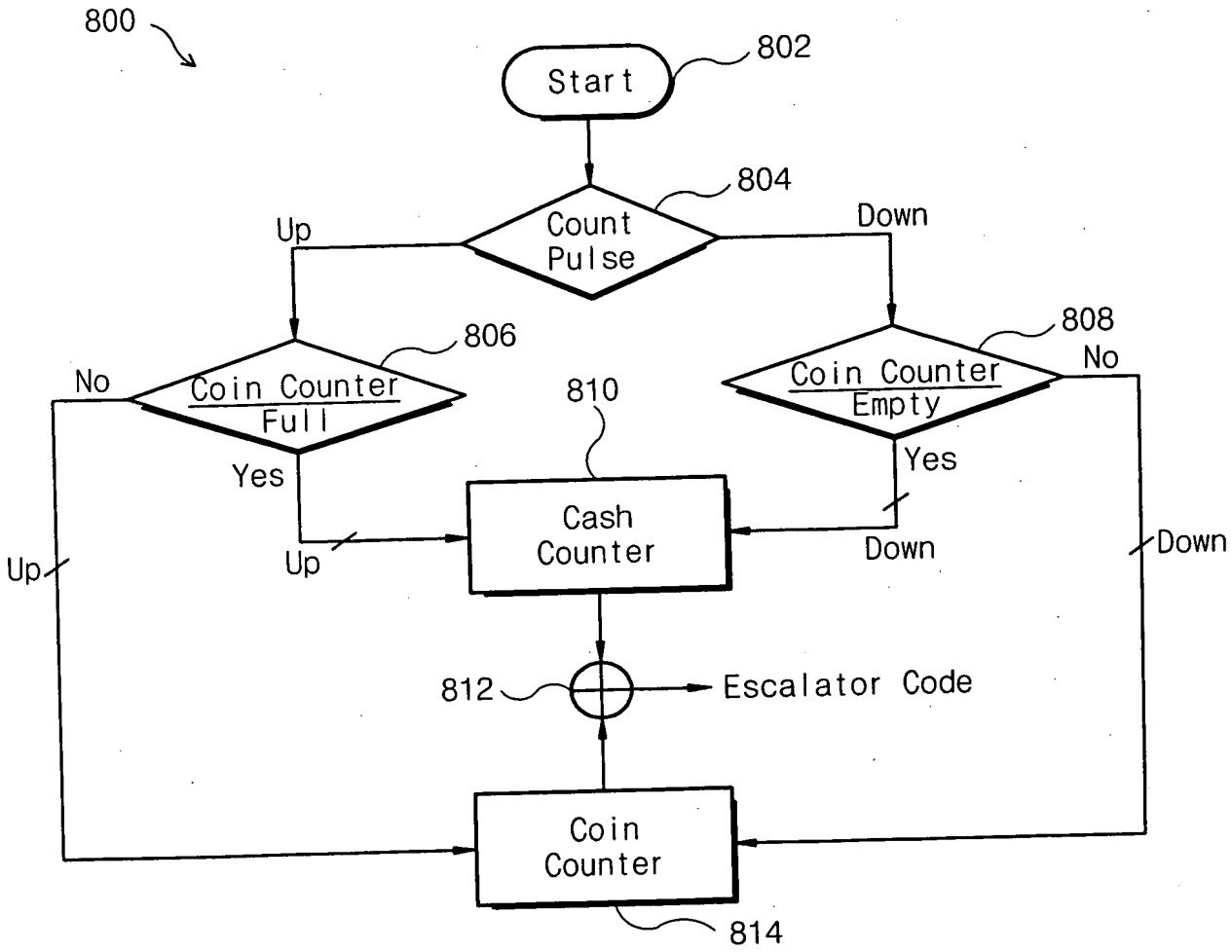

800
Start
802
Count Pulse
804
Up
Down
Coin Counter Full
806
No
Yes
Coin Counter Empty
808
No
Yes
Cash Counter
810
Up
Down
Up
Down
812
Escalator Code
Coin Counter
814

Fig. 9

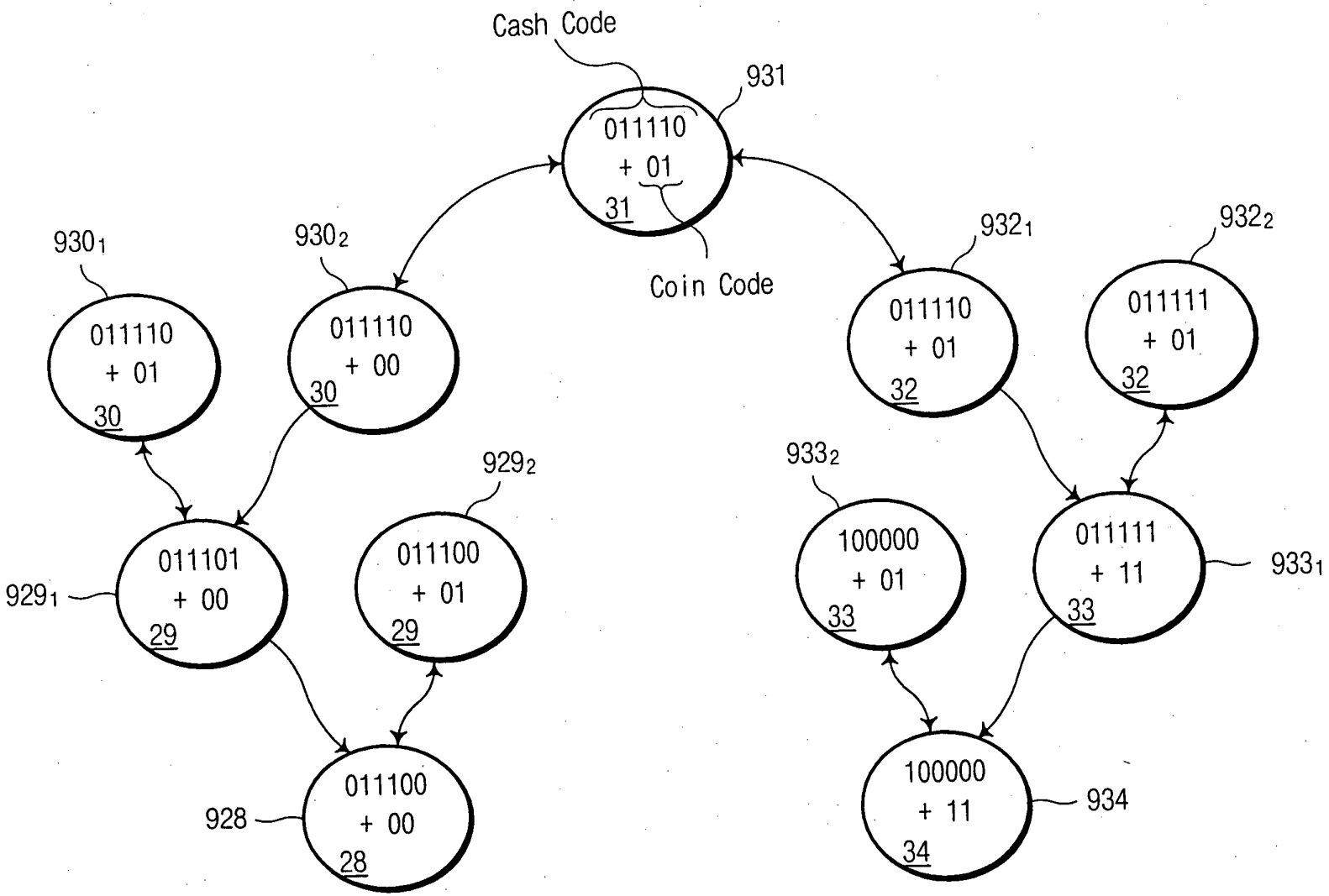

Cash Code
931
011110
+ 01
31
Coin Code
930₁
011110
+ 01
30
930₂
011110
+ 00
30
932₁
011110
+ 01
32
932₂
011111
+ 01
32
929₂
933₂
929₁
011101
+ 00
29
011100
+ 01
29
100000
+ 01
33
011111
+ 11
33
933₁
928
011100
+ 00
28
100000
+ 11
34
934

Fig. 10

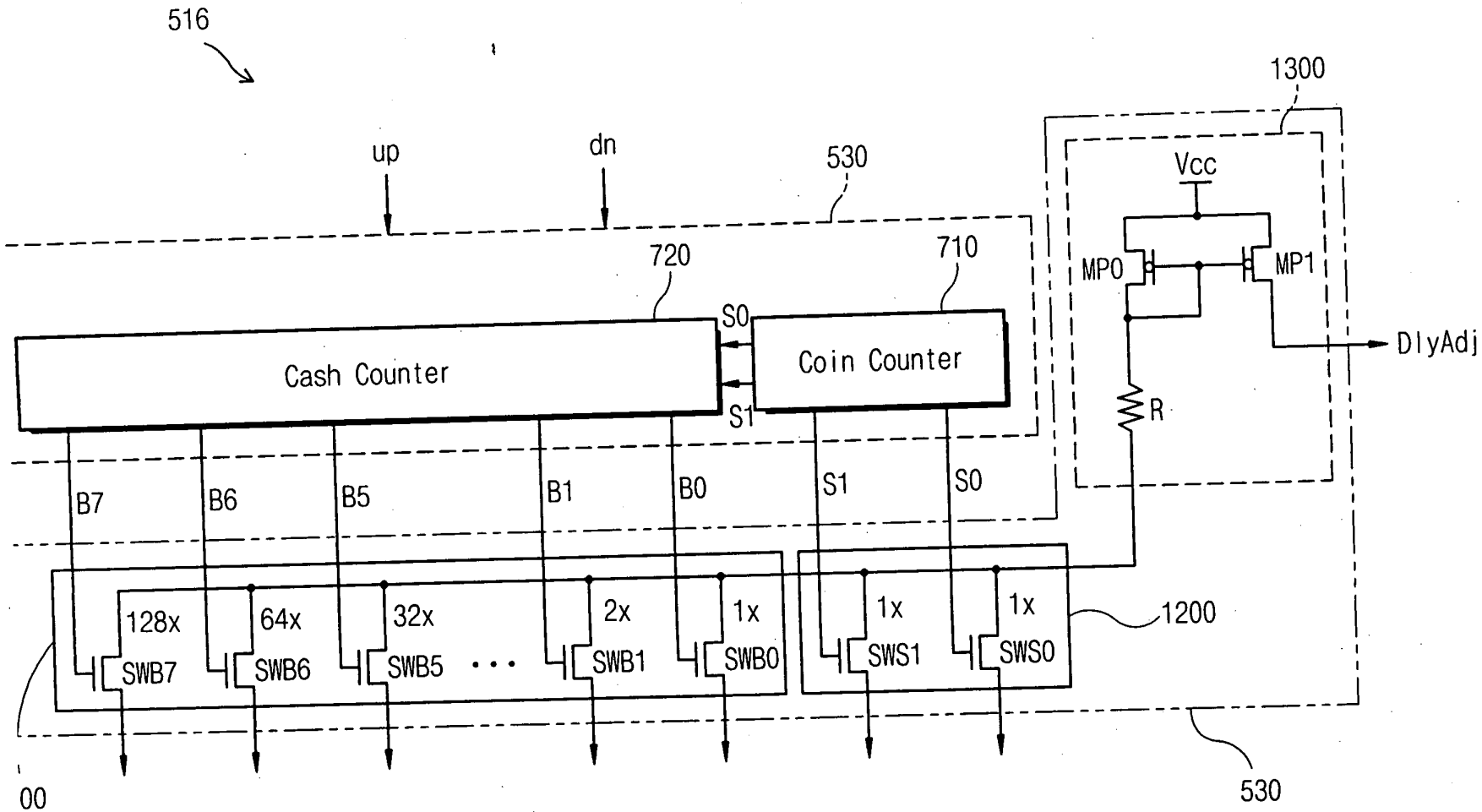

516
1300
up
dn
530
Vcc
720
710
MP0
MP1
S0
Cash Counter
Coin Counter
DlyAdj
S1
R
B7
B6
B5
B1
B0
S1
S0
128x
64x
32x
2x
1x
1x
1x
1200
SWB7
SWB6
SWB5
SWB1
SWB0
SWS1
SWS0
00
530

Fig. 11A

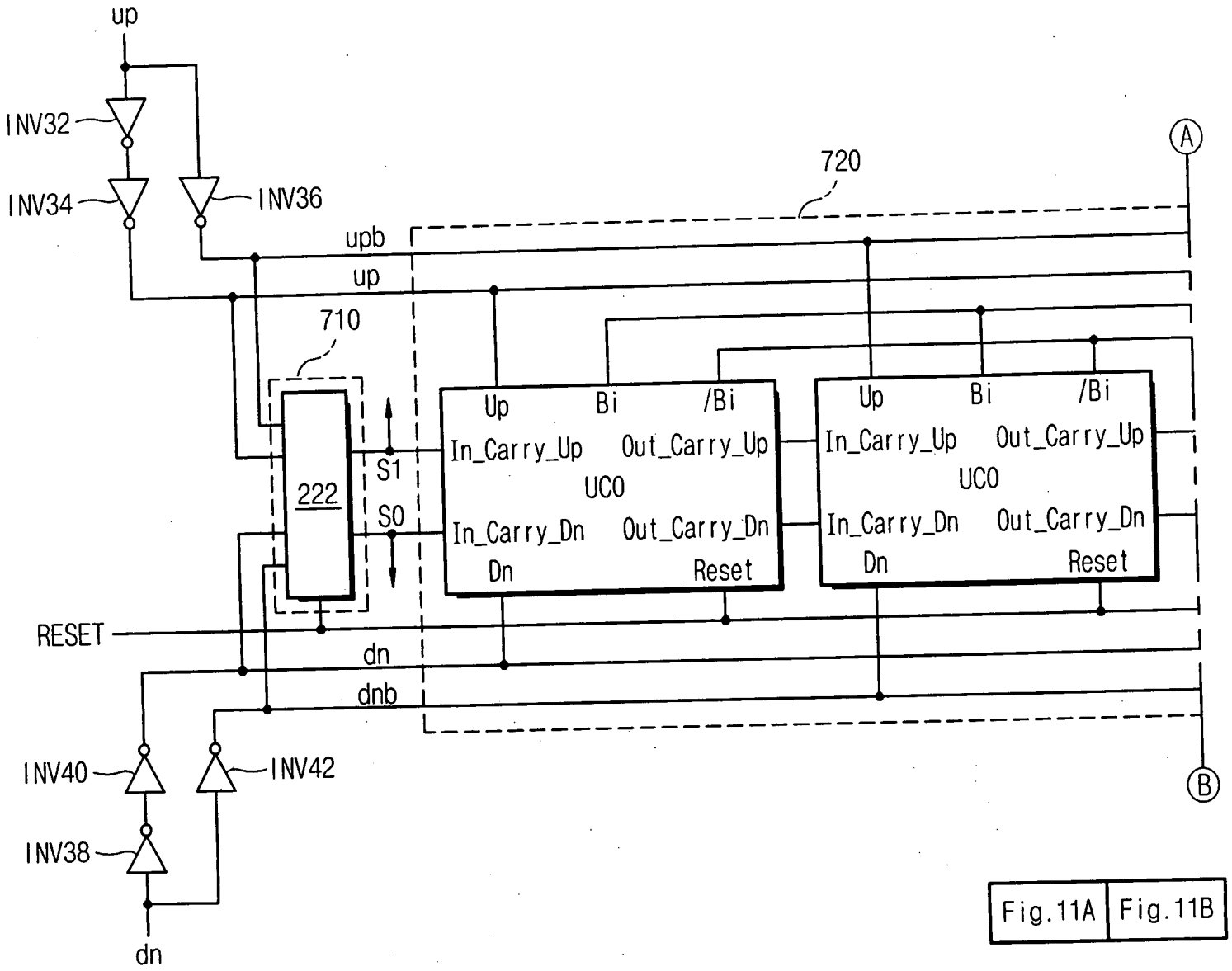


Fig.11A | Fig.11B

Fig. 11B

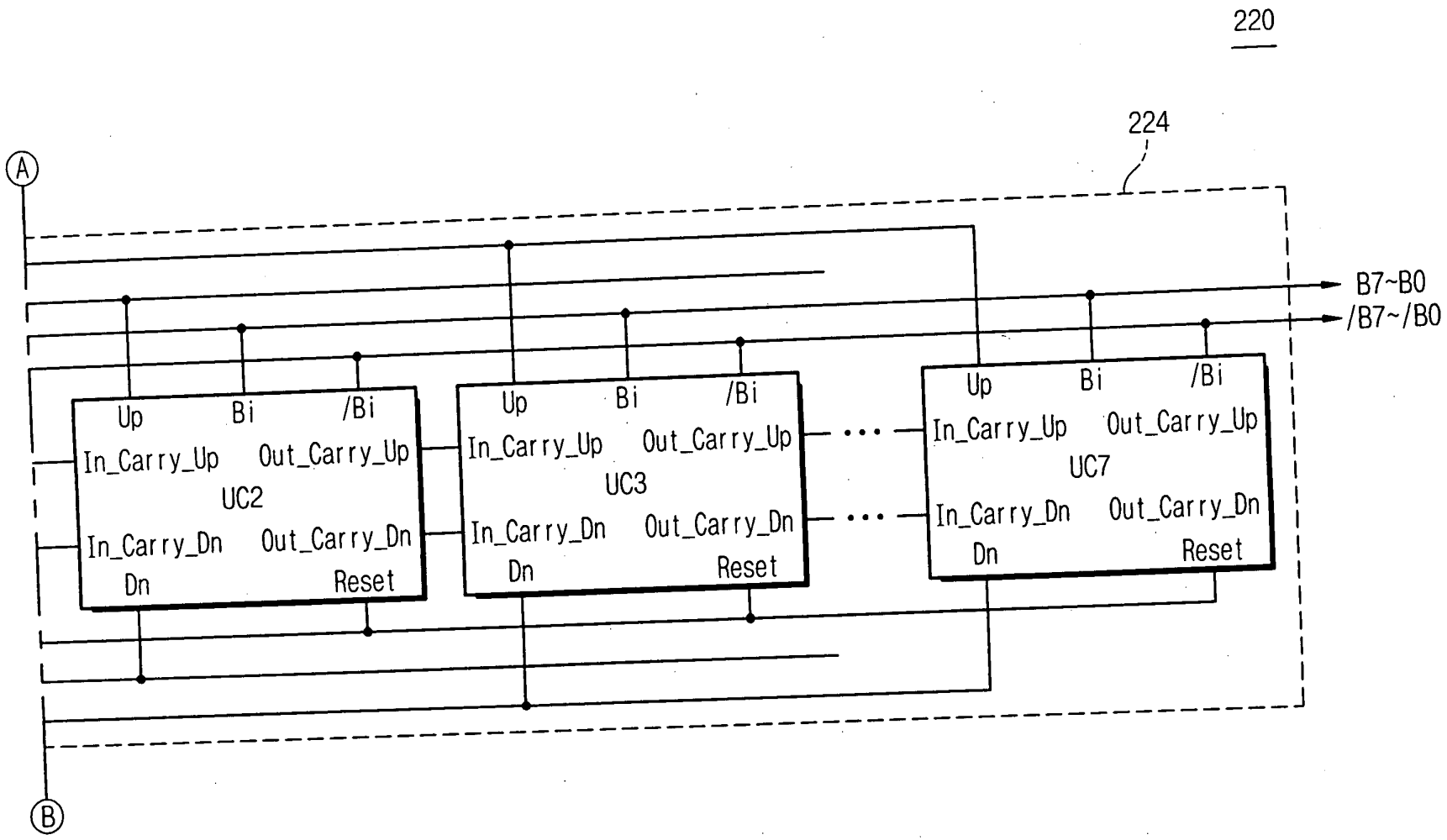

220
224
A
B
Up
Bi
/Bi
In_Carry_Up
Out_Carry_Up
UC2
In_Carry_Dn
Out_Carry_Dn
Dn
Reset
UC3
UC7
B7~B0
/B7~/B0

Fig. 12

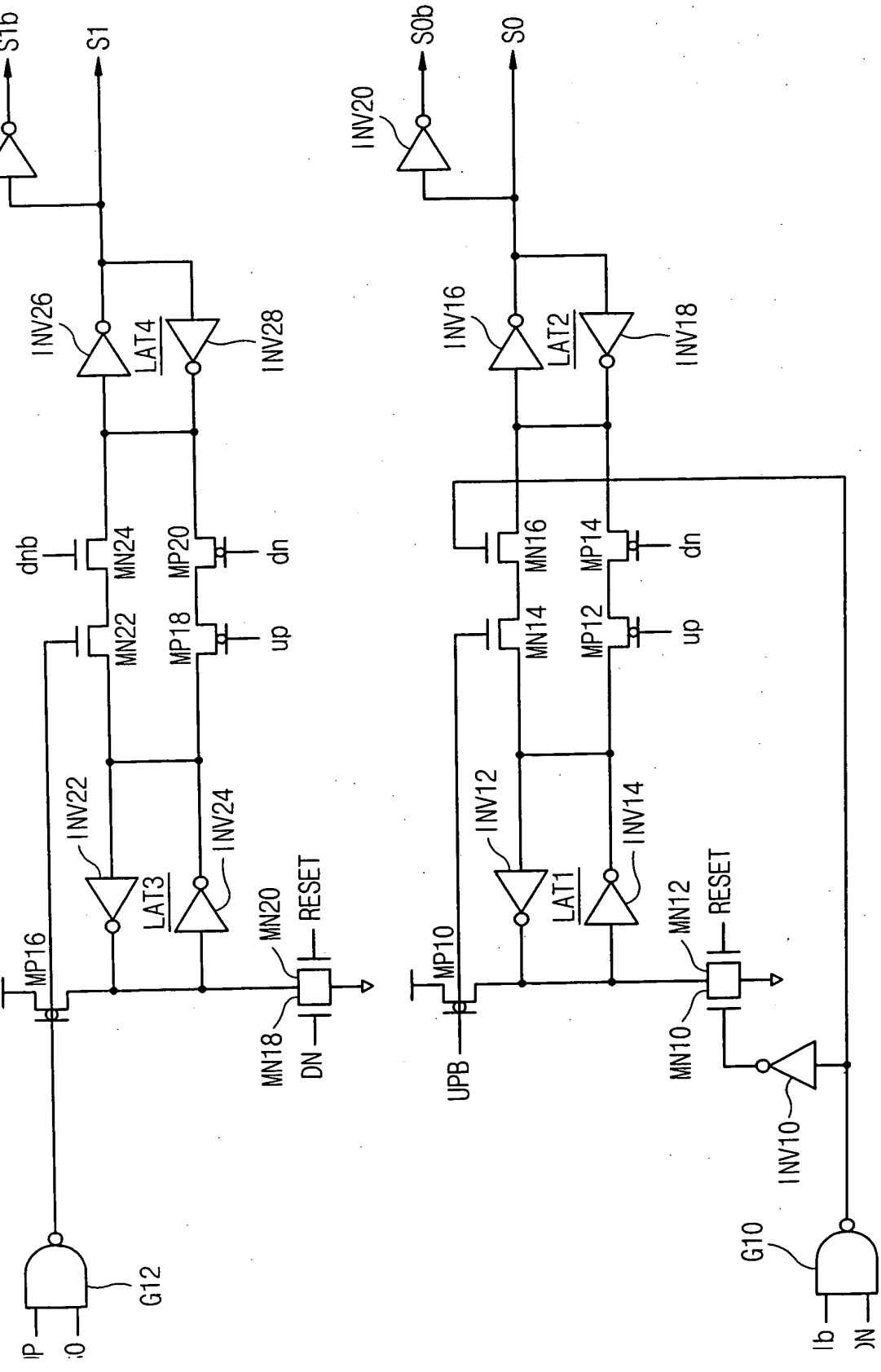

222
S1b
S1
INV30
INV26
LAT4
INV28
dnb
MN24
MP20
dn
MN22
MP18
up
INV22
INV24
LAT3
MP16
MN20
RESET
MN18
DN
G12
S0b
S0
INV20
INV16
LAT2
INV18
MN16
MP14
dn
MN14
MP12
up
INV12
INV14
LAT1
MP10
MN12
RESET
UPB
MN10
INV10
G10

Fig. 13

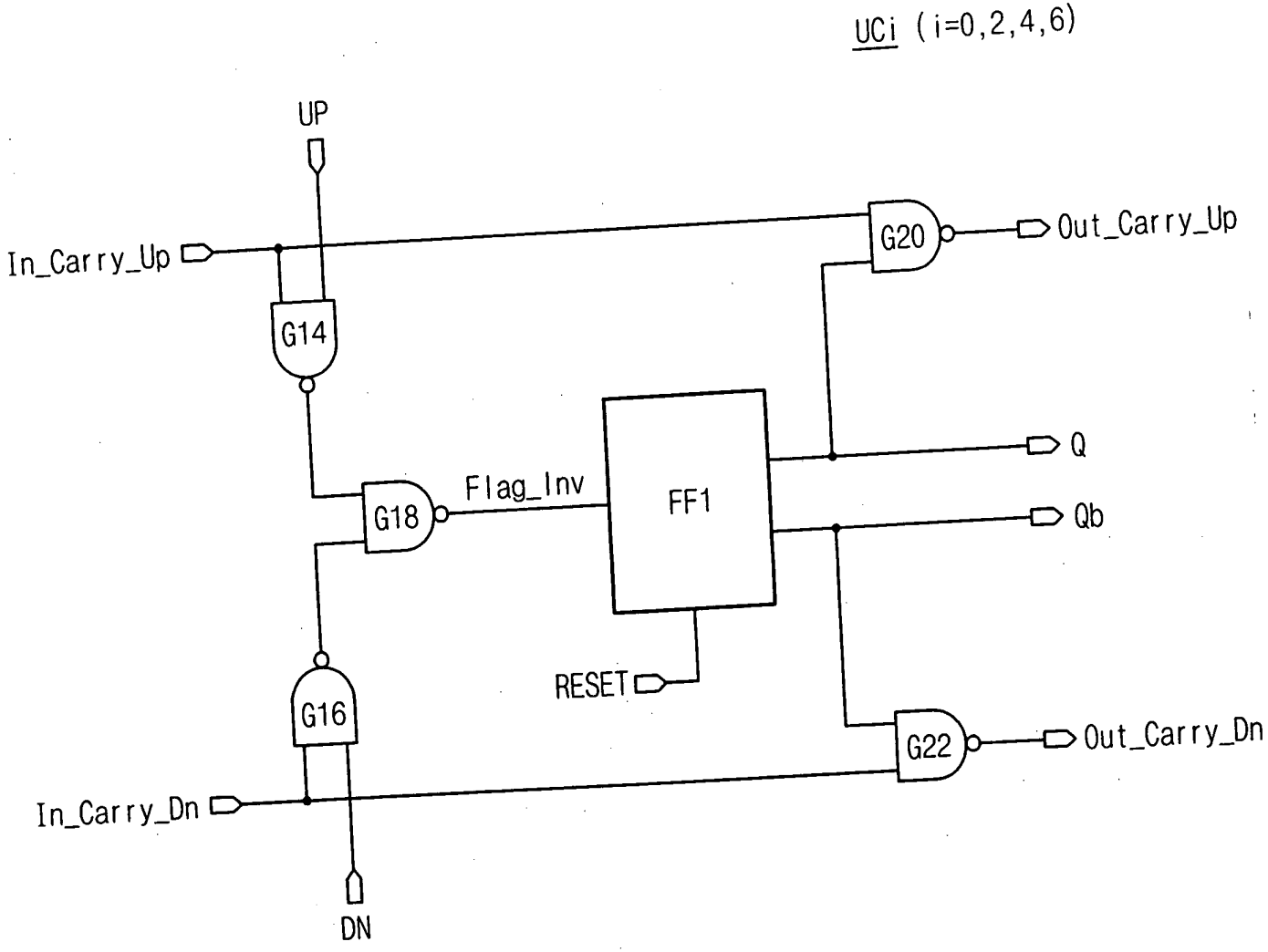

UCi (i=0,2,4,6)
UP
In_Carry_Up
G14
G20
Out_Carry_Up
Q
Qb
G18
Flag_Inv
FF1
RESET
G16
G22
Out_Carry_Dn
In_Carry_Dn
DN

Fig. 14

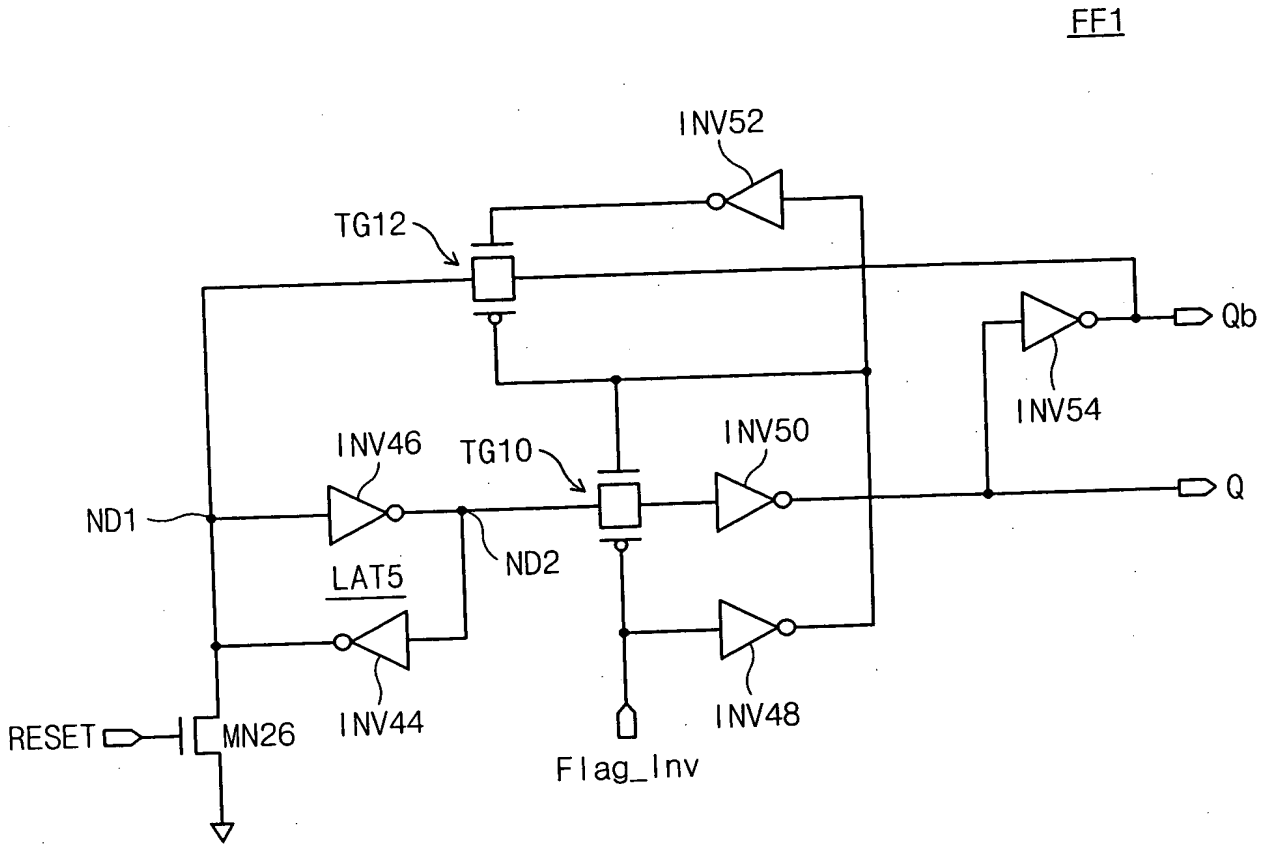

FF1
INV52
TG12
Qb
INV54
INV46
TG10
INV50
ND1
Q
ND2
LAT5
RESET
MN26
INV44
INV48
Flag_Inv

Fig. 15

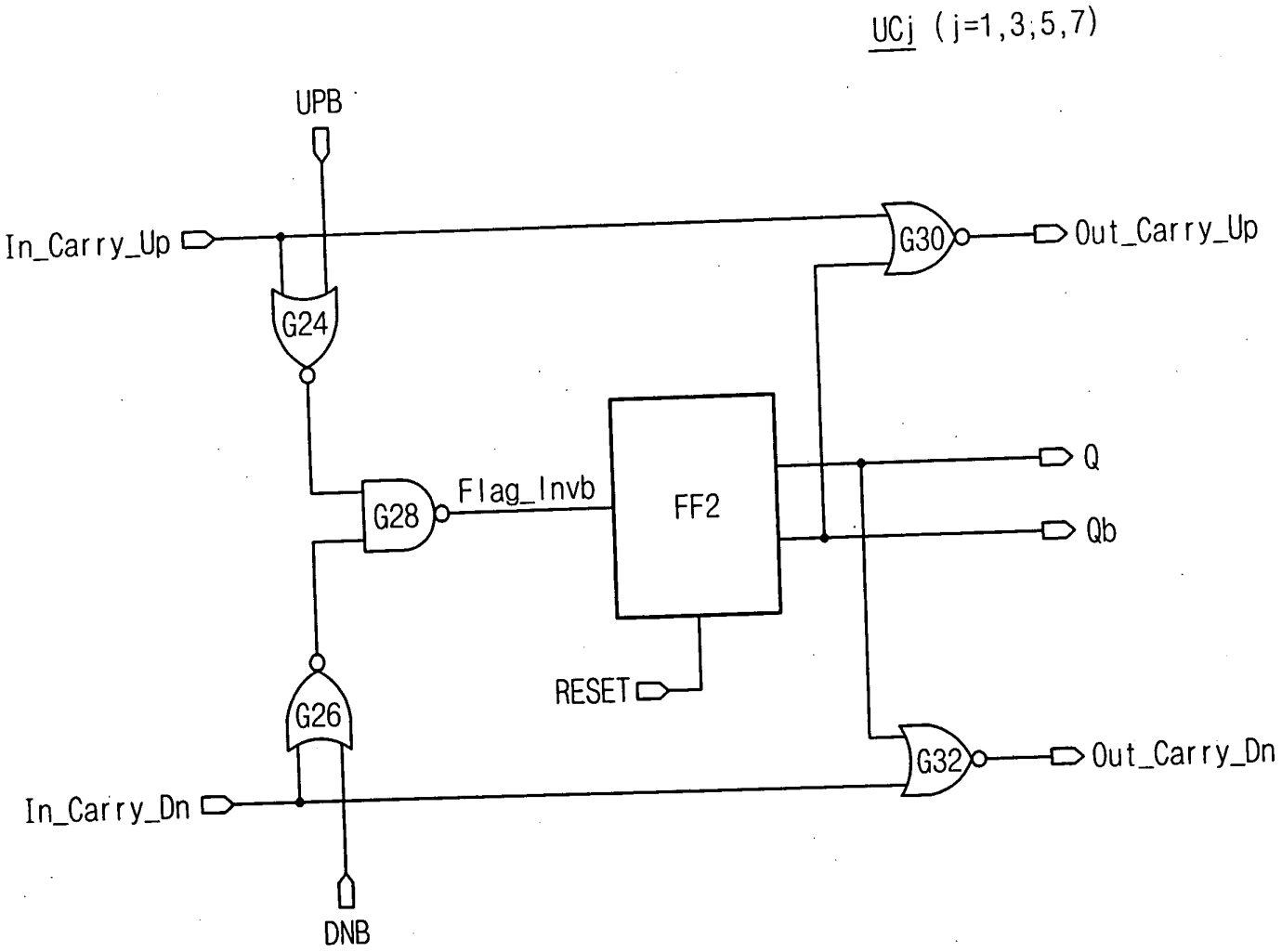

UCj (j=1,3,5,7)
UPB
In_Carry_Up
G24
G30
Out_Carry_Up
G28
Flag_Invb
FF2
Q
Qb
RESET
G26
G32
Out_Carry_Dn
In_Carry_Dn
DNB

Fig. 16

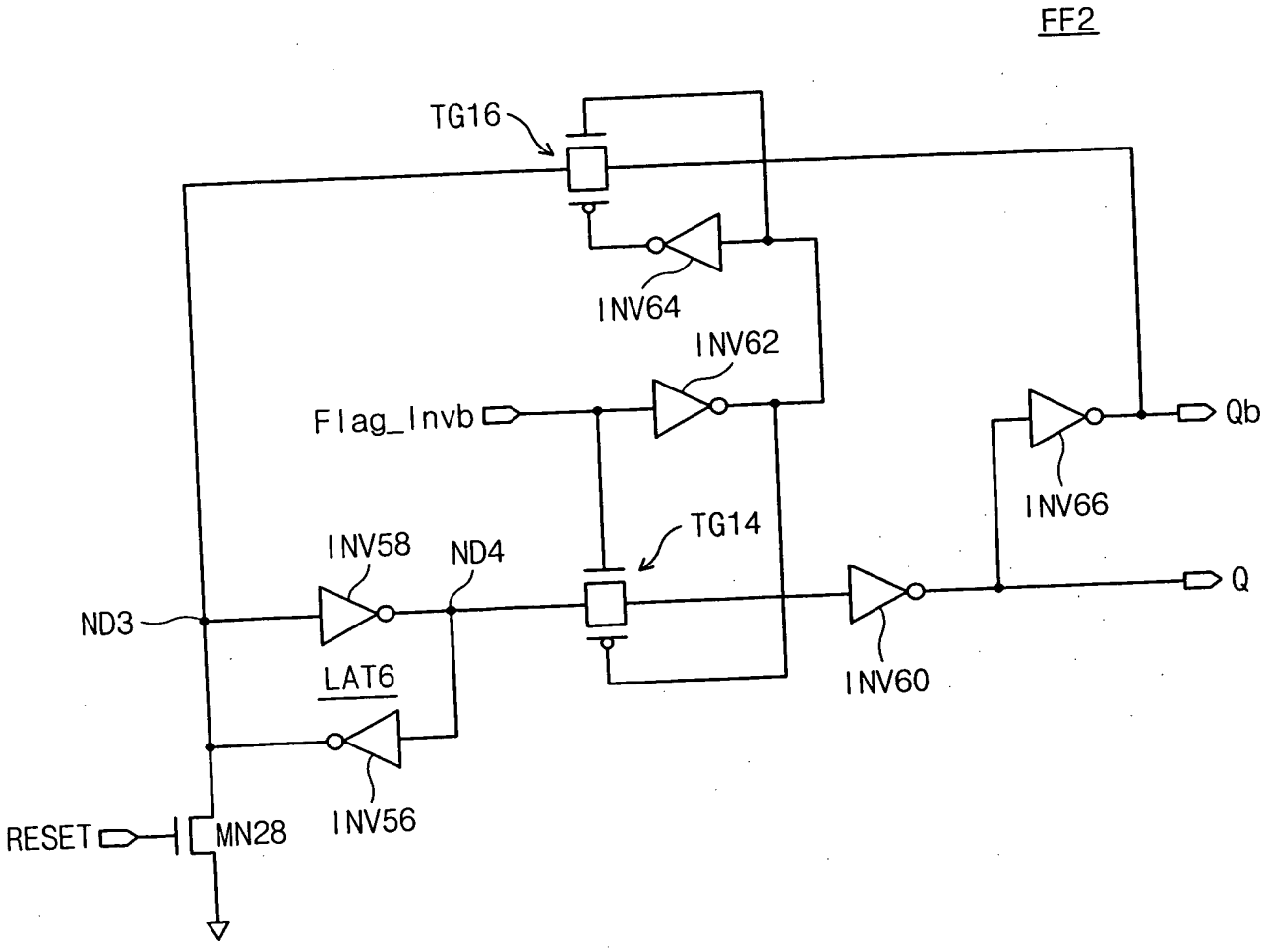

FF2
TG16
INV64
INV62
Flag_Invb
Qb
INV66
TG14
INV58
ND4
Q
ND3
INV60
LAT6
INV56
RESET
MN28

Fig. 17

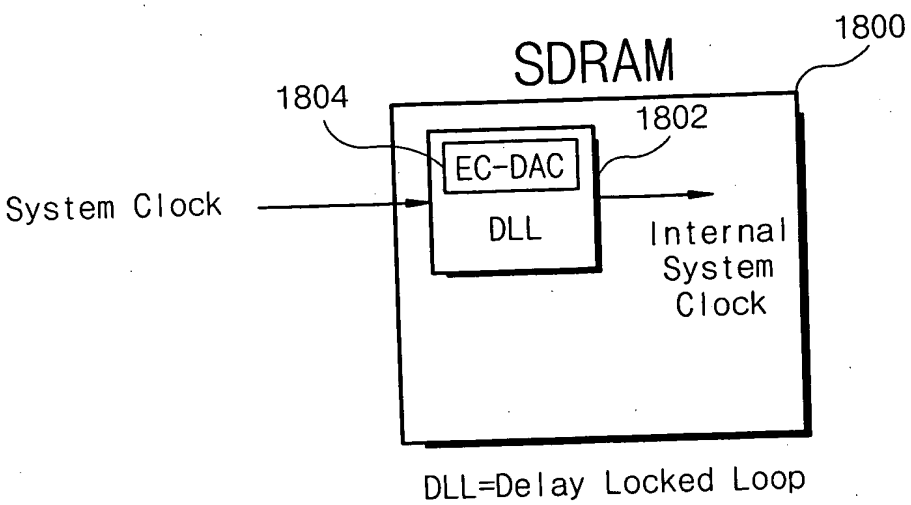
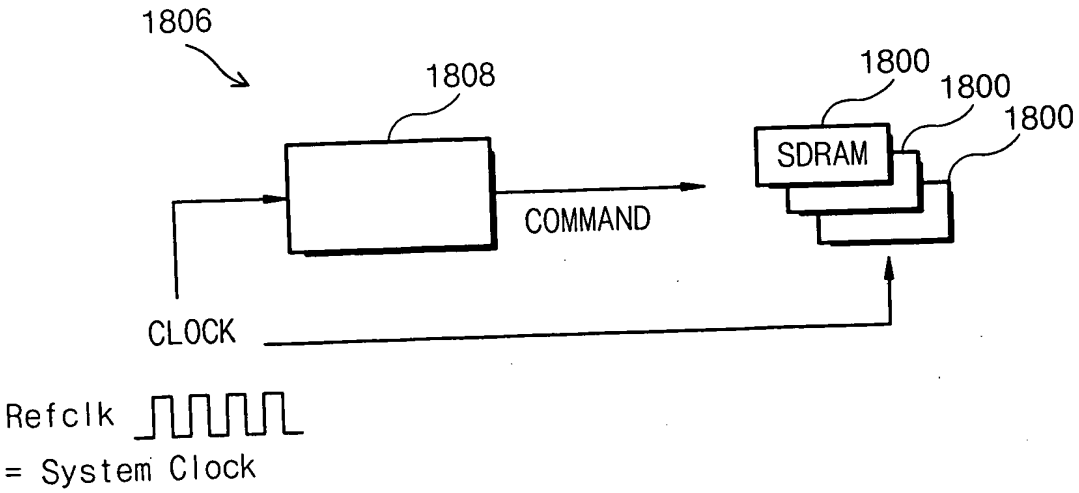

SDRAM
1800
1804
1802
EC-DAC
DLL
System Clock
Internal System Clock
DLL=Delay Locked Loop

Fig. 18


1806
1808
1800
1800
1800
SDRAM
COMMAND
CLOCK
Refclk
= System Clock